AMD

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Application Note

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This application note provides a description of how to replace the Level One LXT970A with the AMD Am79C874 NetPHY-1LP device. A brief comparison of the functionality of the two devices is presented, along with a detailed pin-by-pin comparison. A description of the replacement or elimination of external passive components is also provided. Finally, there is a description of how to use the NetPHY-1LP device with the Motorola MPC860T PowerQUICC™ Fast Ethernet controller.

PRODUCT COMPARISON

A comparison of Am79C874 NetPHY-1LP features and LXT970A features is presented in Table 1.

Table 1. Feature Comparison

Feature	LXT970A	NetPHY-1LP
Power supply	5 V (3.3 V MII optional)	3.3 V (5 V I/O tolerant)
Package	64-lead TQFP	80-lead TQFP
Package Size	14 mm x 14 mm	12 mm x 12 mm
Typical Power	45-850 mW	3-325 mW
Power Management	Power down	Power down, idle wire, unplugged
10BASE-T	Yes	Yes
100BASE-TX	Yes	Yes
100BASE-FX	Yes	Yes
MII	Yes	Yes
GPSI (7 Wire)	No	Yes
5B Symbol (PCS Bypass)	100 Mbps only	10 Mbps and 100 Mbps
LED Support	Link, TX, RX, COL, Speed	Link, TX, RX, COL, Speed, Duplex
Magnetics	1:1	1:1 or 1.25:1

Pin Comparison

The NetPHY-1LP device and the LXT970A are not pin-for-pin replacements for each other. A new layout of the transceiver area will be required when replacing the LXT970A with the NetPHY-1LP device. However, significant advantages are available to the designer replacing the LXT970A with the NetPHY-1LP device, including additional functionality, smaller footprint, and much lower power operation. In Table 2 and Table 3, the two devices are compared, pin by pin. Where there are differences between the functions of the equivalent pins, those differences are described in the comments.

Note: *Blank comment lines indicate that the pin functions of the two devices are the same.*

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Table 2. NetPHY-1LP and LXT970A Functionally Equivalent Pins

LXT970A Pin Number	LXT970A Pin Name	NetPHY-1LP Pin Number	NetPHY-1LP Pin Name	Comments
1	CRS	42	CRS/10CRS	
2	FDS/MDINT	58/43	LEDDPX/LEDTXB, INTR	In its default configuration on the LXT970A, this pin operates as an indicator of full-duplex operation. By writing a 1 to MR17, the function of this pin becomes a status change interrupt.
3	TRSTE	2,3	ISODEF, ISO	The TRSTE input functions identically to ISODEF at reset. After reset, it functions as ISO.
4	MF4			See *Device Configuration Notes.*
5	MF3			See *Device Configuration Notes.*
6	MF2			See *Device Configuration Notes.*
7	MF1			See *Device Configuration Notes.*
8	MF0			See *Device Configuration Notes.*
9	VCCD			
10	TEST	7	BURN_IN	
11	XO	74	XTL-	
12	XI	75	XTL+	
13	FDE			See *Device Configuration Notes*.
14	CFG0			See *Device Configuration Notes*.
15	MDDIS			See the *MDDIS Signal* section.
16	RESET	8	RST	
17	FIBOP	69	FXT+	
18	FIBON	70	FXT-	
19	VCCT			
20	TREF			Not needed with NetPHY-1LP device.
21	TPOP	77	TX+	
22	GNDT			
23	TPON	78	TX-	
24	VCCA			
25	RBIAS	72	IBREF	10.0 kΩ,1% resistor to ground.
26	GNDA			
27	FIBIP	67	TEST1/FXR+	
28	FIBIN	66	TEST0/FXR-	
29	TPIP	64	RX+	
30	TPIN	63	RX-	
31	GNDR			
32	No Connect			

LXT970A Pin Number	LXT970A Pin Name	NetPHY-1LP Pin Number	NetPHY-1LP Pin Name	Comments
33	CFG1			See *Device Configuration Notes.*
34	PWRDWN	9	PWRDN	
35	No Connect			
36	No Connect			
37	VCCR			
38	LEDS	44	LEDSPD[0]/LEDBTB/ FX_SEL	
39	LEDC	45	LEDCOL/SCRAM_EN	
40	LEDL	48	LEDLNK/LED_10LNK/ LED_PCSBP_SD	
41	LEDT	47	LEDTX/LEDBTB	
42	LEDR	46	LEDRX/LEDSEL	
43	GNDD			
44	MDIO	21	MDIO	
45	MDC	22	MDC	
46	RXD4	31	RX_ER/RXD[4]	Only when the NetPHY-1LP device is in PCS bypass mode.
47	RXD3	23	RXD[3]	
48	RXD2	24	RXD[2]	
49	RXD1	25	RXD[1]	
50	RXD0	26	RXD[0]/10RXD	
51	RX_DV	29	RX_DV	
52	GNDIO			
53	VCCIO			
54	RX_CLK	30	RX_CLK/10RXCLK	
55	RX_ER	31	RX_ER/RXD[4]	
56	TX_ER	32	TX_ER/TXD[4]	
57	TX_CLK	33	TX_CLK/10TXCLK/ PCSBP_CLK	This input is the reference clock, if the XI input of the LXT970A is grounded. See REFCLK comment in Table 3.
58	TX_EN	34	TX_EN/10TXEN	
59	TXD0	37	TXD[0]/10TXD	
60	TXD1	38	TXD[1]	
61	TXD2	39	TXD[2]	
62	TXD3	40	TXD[3]	
63	TXD4	32	TX_ER/TXD[4]	Only when the NetPHY-1LP device is in PCS bypass mode.
64	COL	41	COL/10COL	

Table 3 provides a description of the NetPHY-1LP device pins for which there are no functionally equivalent pins on the LXT970A. These pins provide extended functions beyond those available on the LXT970A.

Table 3. NetPHY-1LP Pins Providing Additional Functionality

Pin	Pin Name	Comment
5	REFCLK	If a crystal is used for clock input, ground this pin through a 1 kΩ resistor. If a crystal is not used, this pin supplies the reference clock. If the XI pin of the LXT970A is grounded, the clock supplied to its TX_CLK input should be connected to this signal.
6	CLK25	This output will provide a 25-MHz clock output, if the CLK25EN pin is pulled to ground through a 50-Ω resistor at the rising edge of RST.
19	GPIO[0]/ 10TXD--/ 7WIRE	This pin provides a capability that is an extension beyond the functionality of the LXT970A. It provides a general purpose I/O pin that may be controlled through the Miscellaneous Features register (MR16).
20	GPIO[1]/ TP125	This pin provides a capability that is an extension beyond the functionality of the LXT970A. It provides a general purpose I/O pin that may be controlled through the Miscellaneous Features register (MR16).
57	LEDSPD[1]/ LEDTXA/ CLK25EN	This pin provides a capability that is an extension beyond the functionality of the LXT970A. It indicates when the interface is operating at 10 Mbps.
62	TEST3/ SDI+	This pin provides a capability that is an extension beyond the functionality of the LXT970A. This pin provides a signal detect input, when operating in 100BASE-FX mode.
68	TEST2	This pin should not be connected.

Device Configuration Notes

In order to save a few pins, the LXT970A requires an external resistive voltage divider to supply two intermediate voltages, for a total of four levels, to the MF4-0 pins that configure the device for operation and provide its address. Each of the MF4-0 inputs control two functions, one of the PHY address bits and one of the MII register configuration bits. The NetPHY-1LP device does not use this method for its configuration, consequently eliminating the need for the voltage divider network and simplifying the configuration of the device. The NetPHY-1LP device utilizes separate pins for configuration and addressing. This section provides a description of how to convert the multilevel configuration signals of the LXT970A to the inputs required to configure the NetPHY-1LP device.

Four voltages are used by the LXT970A to indicate the configuration information supplied via the MF4-0 pins, V_{MF1}, V_{MF2}, V_{MF3}, and V_{MF4}. The voltage values may be thought of as a two-bit binary value, where each bit independently controls either the associated PHY address bit or the MII configuration register bit. Table 4 shows the encoding of the two bits to the control voltage applied to the MF4-0 pins. From Table 4 the appropriate setting for the NetPHY-1LP configuration inputs may be determined.

Table 4. LST970A Control Voltage Encoding

	PHY Address bit = 0	PHY Address bit = 1
Configuration bit = 0	V_{MF4}	V_{MF1}
Configuration bit = 1	V_{MF3}	V_{MF2}

PHY Address Configuration

Table 5 shows the correspondence between the NetPHY-1LP PHYAD[4:0] configuration inputs and the LXT970A MF4-0 configuration inputs. The value of the PHY address bit determined from Table 4 should be applied to the corresponding PHYAD[4:0] input.

Table 5. PHY Address Configuration Inputs

LXT970A Pin Name	NetPHY-1LP Pin Name	NetPHY-1LP Pin Number
MF0	PHYAD[0]	18
MF1	PHYAD[1]	17
MF2	PHYAD[2]	16
MF3	PHYAD[3]	15
MF4	PHYAD[4]	14

Major Function Configuration

Table 6 shows the correspondence between the NetPHY-1LP ANEGA, RPTR, PCSBP, and LEDCOL/SCRAM_EN pins and the LXT970A MF0-4 configuration inputs. The value of the configuration bit determined from Table 4 should be applied to the corresponding input of the NetPHY-1LP device, as shown in Table 6.

Table 6. Major Function Configuration Inputs

LXT970A Pin Name	NetPHY-1LP Pin Name	NetPHY-1LP Pin Number
MF0	ANEGA	56
MF1	RPTR	61
MF2	PCSBP	1
MF3	LEDCOL/ SCRAM_EN	45
MF4	See Auto-Negotiation and 100BASE-FX Selection section	

Auto-Negotiation and 100BASE-FX Selection

The MF4 pin controls disparate functions, depending on the setting of Auto-Negotiation. If Auto-Negotiation is disabled by MF0, MF4 controls the selection of 100BASE-TX or 100BASE-FX operation. In this case, the function of MF4 corresponds to the absence or presence of a pull-down resistor on the LEDSPD[0]/LEDBTB/FX_SEL input, pin 44, of the NetPHY-1LP device. When the configuration bit is 1, the pull-down resistor should be connected to the LEDSPD[0]/LEDBTB/FX_SEL input, to enable 100BASE-FX operation. If Auto-Negotiation is enabled by MF0, the function of MF4 is combined with the CFG1 and FDE inputs to determine the capabilities advertised during the Auto-Negotiation phase. Table 7 shows the correspondence of MF4, CFG1, and FDE on the LXT970A to the TECH_SEL[2:0] inputs of the NetPHY-1LP device, when Auto-Negotiation is enabled. The value of the MF4 bit is for the configuration function only.

MDDIS Signal

The LXT970A provides a signal named MDDIS to disable the management interface. When this signal is active, MDIO is read-only and the MII configuration register bits are controlled continuously by the MF4:0, CFG1:0, and FDE input signals. *There is no equivalent mode of operation in the NetPHY-1LP device*.

Table 7. Auto-Negotiation and 100BASE-FX Selection

LXT970A MF4, CFG1, FDE	NetPHY-1LP TECH_SEL [2:0]	Capabilities Advertised
00X	111	All capabilities advertised
010	001	10 Mbps only, half-duplex
011	101	10 Mbps only, full duplex and half-duplex
100	010	100 Mbps only, half-duplex
101	110	100 Mbps only, full duplex and half-duplex
110	011	10 and 100 Mbps, half-duplex
111	111	10 and 100 Mbps, full duplex and half-duplex

The MDDIS pin is also used to control the default state of the bits controlled by the MF4:0, CFG1:0, and FDE input signals. If MDDIS is low at reset, the default configuration is loaded into the appropriate MII registers and the MDIO interface is enabled. This is equivalent to the operation of the NetPHY-1LP device at reset, when the TECH_SEL[2:0] inputs are used to configure the device.

Management Registers

The management registers of the NetPHY-1LP device are identical to those of the LXT970A, with the following exceptions:

1. In the Auto-Negotiation Advertisement Register (MR4), bit 15 is used by the Am79C874 device to enable and disable the next page capability. The LXT970A does not support this feature. Also in this register, bit 14 is reserved in the LXT970A. This bit provides an acknowledgement indication in the NetPHY-1LP device, after three consecutive and consistent FLP bursts are received. Bit 10 in this register is used by the LXT970A to enable pause operation for full-duplex links. This capability is *not* supported by the Am79C874 device.
2. In the Auto-Negotiation Link Partner Ability Register (MR5), the LXT970A uses bit 10 to indicate the link partner's pause operation capability. This function is *not* supported by the Am79C874 device.
3. In the Auto-Negotiation Expansion Register (MR6), bit 2 is permanently set to zero in the LXT970A to indicate that the next page function is not supported. This bit is permanently set to one in the Am79C874 device to indicate that this function is supported.

4. The Auto-Negotiation Next Page Advertisement register (MR7) does not exist in the LXT970A. The Am79C874 device includes this register to send the next page message. See the Am79C874 NetPHY-1LP data sheet for details.
5. The Miscellaneous Features register (MR16) controls a number of different features of the Am79C874 device. This register is used as a Mirror register in the LXT970A. See the Am79C874 NetPHY-1LP data sheet for details.
6. The Interrupt Control/Status register (MR17) is significantly different in the LXT970A and the Am79C874 device. The LXT970A uses this register as a global interrupt enable and to control MII driver levels and link up/down criteria. The Am79C874 device uses this register to individually enable each interrupt source and to indicate the status of the interrupt sources. See the Am79C874 NetPHY-1LP data sheet for details.
7. The LXT970A Diagnostic register (MR18) is significantly different from the Am79C874 device Diagnostic register (MR18). The LXT970A uses this register as a global interrupt status register and to indicate that the device is powered up and its clocks are stable. The Am79C874 device uses this register to indicate the result of Auto-Negotiation for duplex and speed, as well as to indicate that the receiver is locked and has received data from the link.
8. The Am79C874 device uses MR19 as the Power/Loopback register. Its functions are to control operation of the loopback tests, control low power operation, control use of a 1.25:1 transformer, and to control the Auto-Negotiation timer value. The LXT970A uses this register as a configuration register. The following bits have equivalent functions in the Am79C874 device:
    a. Bit 13 of the LXT970A register is equivalent to bit 15 in MR16 of the Am79C874 device. This bit controls the repeater mode.
    b. Bit 11 of the LXT970A register is equivalent to bit 10 in MR16 of the Am79C874 device. This bit controls the 10BASE-T loopback mode.
    c. Bit 10 of the LXT970A register is equivalent to bit 11 in MR16 of the Am79C874 device. This bit controls the 10BASE-T SQE mode.
    d. Bit 9 of the LXT970A register is equivalent to bit 12 in MR21 of the Am79C874 device. This bit controls the 10BASE-T jabber mode.
    e. Bit 4 of the LXT970A register is equivalent to bit 1 in MR21 of the Am79C874 device. This bit controls the PCS bypass mode.
    f. Bit 3 of the LXT970A register is equivalent to bit 2 in MR21 of the Am79C874 device. This bit controls the scrambler mode.
    g. Bit 2 of the LXT970A register is equivalent to bit 0 in MR21 of the Am79C874 device. This bit controls the 100BASE-FX mode.
    h. Other bits of the LXT970A register are either reserved or have no functional equivalent in the Am79C874 device.
9. The Chip Status register (MR20) of the LXT970A indicates the status of various functions. It does *not* have a functional equivalent in the Am79C874 device.
10. The following registers do *not* have equivalents in the LXT970A (see the Am79C874 NetPHY-1LP data sheet for details):
    a. Disconnect Counter (MR23)
    b. Receive Error Counter (MR24)

Passive Components

The passive components used by both devices for serial termination of the MII and pull-up of the LEDs are identical, as are the termination resistors for the twisted pair inputs and outputs when a 1:1 transformer is used. The termination resistors should be changed to 78.1 Ω, when a 1.25:1 transformer is used.

For 100BASE-FX operation, the resistive termination must be changed. When a 3.3-V fiber-optic transceiver is used, follow the recommended termination shown in the Am79C874 NetPHY-1LP data sheet. Note that fiber-optic transceiver vendors may have different recommendations for receive-pair termination on their side of the receive-pair capacitors.

When a 5-V fiber-optic transceiver is used, it may be possible to eliminate the receive-pair capacitors and the termination resistors on the fiber-optic transceiver side. The transmit-pair should be terminated via 82-Ω resistors to 5 V and 130-Ω resistors to ground. The NetPHY-1LP device SDI+ pin should have a 301-Ω resistor to ground and a 200-Ω series resistor between the 301-Ω resistor and the SD pin on the fiber-optic transceiver.

The bias resistor connected to the RBIAS pin of the LXT970A should be replaced with a 10.0-kΩ 1% resistor connected to the IBREF pin of the NetPHY-1LP device.

If the default configuration provided by the NetPHY-1LP pins is desired, many of the configuration pins may be left unconnected. The NetPHY-1LP device includes internal resistors on the configuration inputs which allow the designer to leave these pins unconnected when selecting the default function of the pin. The pins with internal resistors are shown in Table 8.

Table 8. NetPHY-1LP Pins with Internal Resistors

Pin	Name	Resistor	Function
1	PCSBP	Pull down	Disables PCS bypass function
2	ISODEF	Pull down	Enables the MII output pins by default
3	ISO	Pull down	Enables the MII output pins
7	BURN_IN	Pull down	Burn-in test is disabled
8	RST	Pull up	Disables reset
9	PWRDN	Pull down	Normal operation is selected
14	PHYAD[4]	Pull up	PHYAD[4] = 1
15	PHYAD[3]	Pull up	PHYAD[3] = 1
16	PHYAD[2]	Pull up	PHYAD[2] = 1
17	PHYAD[1]	Pull up	PHYAD[1] = 1
18	PHYAD[0]	Pull up	PHYAD[0] = 1
19	GPIO[0]	Pull up	Standard MII operation is selected at reset
20	GPIO[1]	Pull down	1:1 transformer operation is selected at reset
21	MDIO	Pull down	Requires external 1.5 kΩ pull up
44	LEDSPD[0]	Pull up	100BASE-TX operation is selected at reset
45	LEDCOL	Pull up	Scrambler operation is enabled at reset
46	LEDRX	Pull up	Standard LED operation is selected at reset
53	TECH_SEL[2]	Pull up	TECH_SEL[2] = 1
54	TECH_SEL[1]	Pull up	TECH_SEL[1] = 1
55	TECH_SEL[0]	Pull up	TECH_SEL[0] = 1
56	ANEGA	Pull up	Enable Auto-Negotiation
57	LEDSPD[1]	Pull up	Disables 25-MHz clock output on CLK25 pin at reset

Note: *The default values for the TECH_SEL[2:0] inputs cause the NetPHY-1LP device to advertise all capabilities during Auto-Negotiation.*

Additional NetPHY-1LP Functions

The NetPHY-1LP device provides five significant enhanced functions beyond those of the Level One LXT970A. These functions are enhanced power management, 7-wire General Purpose Serial Interface (GPSI) for 10BASE-T operation, 5B Symbol MAC interface, enhanced LED operation, and operation with a 1.25:1 transformer.

Enhanced Power Management

The NetPHY-1LP device provides significantly better power management than the LXT970A. The LXT970A has a single low-power operating state, controlled by the PWRDWN pin. In this state, only the MDIO interface is operating. This state is equivalent to the state the NetPHY-1LP device enters when its PWRDN pin is activated. The NetPHY-1LP device has two additional low-power operating states. When the link cable is unplugged, the NetPHY-1LP device will be reduced to approximately 33% of its typical power dissipation. When the link is idle, the NetPHY-1LP device will be reduced to approximately 90% of its typical power dissipation.

7-Wire GPSI MAC Interface

7-Wire GPSI operation of the NetPHY-1LP device is selected when the GPIO[0]/10TXD--/7-Wire pin is pulled to ground through a 10-kΩ resistor. This enables the GPSI MAC interface on the RXD[0]/10RXD, RX_CLK/10RXCLK, TX_CLK/10TXCLK/PCSBP_CLK, TX_EN/10TXEN, TXD[0]/10TXD, COL/10COL, and CRS/10CRS pins. In this mode, the NetPHY-1LP device may be used with MAC chips that implement the GPSI, such as the Motorola QUICC™ and PowerQUICC™ microprocessors.

5B Symbol MAC Interface

The NetPHY-1LP device provides a serial differential interface for use with the Intel/DEC 21143 MAC in the internal SIA (10BASE-T) mode. In this mode, the NetPHY-1LP device operates as a 10BASE-T transceiver, providing received data to the 21143 over a serial differential pair. The 21143 uses two serial differential pairs to provide transmit data to the NetPHY-1LP device, where the two differential pairs are combined in the NetPHY-1LP device to compensate for inter-symbol interference on the twisted-pair medium.

Advanced LED Functions

The NetPHY-1LP device provides advanced LED functions when the LEDRX/LEDSEL pin is pulled low through a 2.5-kΩ resistor. The advanced LED functions provide the same information as the standard LED functions, using fewer LEDs. Dual-color LEDs are used in this mode to indicate transmit and receive activity, duplex status, and speed of a link using only two LEDs.

1.25:1 Transformer

When the GPIO[1]/TP125 pin is pulled high through a 10-kΩ resistor, twisted-pair operation with a 1.25:1 transformer is selected. In this mode, the transmit section of the NetPHY-1LP device dissipates 20% less power when operating, resulting in a 10% overall reduction of power dissipation. When this mode is

selected, the transmit termination resistors must be changed to 78.1-Ω 1% resistors.

Using the NetPHY-1LP Device with a Motorola MPC860T

The Motorola MPC860T PowerQUICC™ Fast Ethernet controller provides a highly functional, microprocessor-based controller incorporating 100BASE-TX/FX, 10BASE-T, and wide area network (WAN) capabilities. The NetPHY-1LP device is a perfect Ethernet transceiver to use with this controller. This section describes the connection of the NetPHY-1LP device to the MPC860T and the programming of the MPC860T to configure its interface to the NetPHY-1LP device.

Connection of the NetPHY-1LP Device to the MPC860T

The connection of the NetPHY-1LP device to the MPC860T is very straightforward. The IEEE 802.3 compliant MII is used to transfer, receive, and transmit data, clock, control, and management information between the two devices.

To enable the MII interface on the MPC860T, a 1 must be written to bit 29 of the R_CNTRL register (address 0F36H). In the MPC860T, the pin used for the MII_TX_CLK is also the IRQ7 interrupt input. Enabling the MII function of this pin does not disable its interrupt function. The interrupt must be disabled or it will constantly be active. This interrupt may be disabled by writing to the SIMASK register (address 14h) of the MPC860T and setting bit 14 = 0.

The NetPHY-1LP device may be configured in its default condition by leaving all configuration pins unconnected. This will enable the MII interface, configure the NetPHY-1LP device for 100BASE-T operation, advertise all capabilities during Auto-Negotiation, set the PHY address to all 1s, and select a 1:1 transformer. If a different configuration is desired, see the Am79C874 NetPHY-1LP data sheet for details

Table 9. NetPHY-1LP and MPC860 Pin Connections

NetPHY-1LP Pin Number	NetPHY-1LP Pin Name	MPC860T Pin Number	MPC860T Pin Name
21	MDIO	H18	MII_MDIO
22	MDC	R16	MII_MDC
23	RXD[3]	U17	MII_RXD3
24	RXD[2]	V19	MII_RXD2
25	RXD[1]	V18	MII_RXD1
26	RXD[0]	W18	MII_RXD0
29	RX_DV	V16	MII_RX_DV
30	RX_CLK	W17	MII_RX_CLK
31	RX_ER	T15	MII_RX_ER
32	TX_ER	T16	MII_TX_ER
33	TX_CLK	W18	MII_TX_CLK
34	TX_EN	V15	MII_TX_EN
37	TXD[0]	V17	MII_TXD0
38	TXD[1]	W16	MII_TXD1
39	TXD[2]	U16	MII_TXD2
40	TXD[3]	U15	MII_TXD3
41	COL	H4	MII_COL
42	CRS	B7	MII_CRS